Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (Currently Amended) A memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests;

a memory interface, for connection to a memory device over a memory bus;

a plurality of buffers in the memory interface; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, each of said multiple data bursts is assigned by the control logic to a respective buffer of the plurality of buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in the respective buffer, and

wherein, for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic, the beginning and end data for the memory access request being [[and]] stored in the single respective sub-buffers buffer by the memory interface, the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data, and

wherein the control logic records a value of a pointer indicating a first sub-buffer of the single buffer storing the end data, such that the control logic is able to return to the indicated sub-buffer to retrieve the end data from the single buffer.

2.   (Previously Presented) A memory controller as claimed in claim 1, wherein, when returning data to the respective device from which a memory access request

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requiring multiple data bursts over the memory bus was received, data is read out from a first part of the single buffer, then data is read out from at least one other of said buffers, then data is read out from a second part of the single buffer.

Claims 3-4.   (Canceled)

5.   (Original) A memory controller as claimed in claim 1, wherein the control logic determines whether a received read access request is a wrapping request which requires multiple memory bursts, and, if so, the control logic allocates each of said memory bursts to a respective one of said buffers.

6.   (Original) A memory controller as claimed in claim 1, wherein the memory controller is a SDRAM controller, and said memory interface is suitable for connection to a SDRAM memory device over said memory bus.

7.   (Currently Amended) In a memory controller including at least one bus interface for connection to at least one respective device for receiving memory access requests, a memory interface for connection to a memory device over a memory bus, a plurality of buffers in the memory interface, and control logic for placing received memory access requests into a queue of memory access requests, a method of retrieving data comprising:

in response to a received memory access request requiring multiple data bursts over the memory bus, assigning each data burst to a respective buffer in a plurality of buffers in the memory interface; and

storing data from each of said multiple data bursts in the respective buffer in the memory interface: [[,]]

wherein, for a wrapping memory access request, assigning data required for a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic and to be stored in the respective sub-buffers of the single respective buffer in the memory interface, the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data,

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<u>recording a value of a pointer indicating a first sub-buffer of the single buffer</u>
<u>storing the end data, and</u>

<u>using the pointer to return to the indicated sub-buffer to retrieve the end data.</u>

8.   (Previously Presented) A method as claimed in claim 7, further
comprising, when returning data to the respective device from which a memory access request
requiring multiple data bursts over the memory bus was received, reading data out from a first
part of single buffer, then reading data out from at least one other of said buffers, then reading
data out from a second part of the single buffer.

Claims 9 - 10. (Canceled)

11.   (Previously Presented) A method as claimed in claim 7, further
comprising determining whether a received read access request is a wrapping request which
requires multiple memory bursts, and, if so, performing the step of assigning each of said data
bursts to a respective one of said buffers.

12.   (Original) A method as claimed in claim 7, wherein the memory controller
is a SDRAM controller, and said memory interface receives data from a SDRAM memory
device over said memory bus in SDRAM bursts.

13.   (Currently Amended) A programmable logic device, wherein the
programmable logic device includes a memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one
respective device formed within the programmable logic device for receiving memory access
requests;

a memory interface, for connection to an external memory device over a memory
bus;

a plurality of buffers in the memory interface; and

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control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, each of said multiple data bursts is assigned by the control logic to a respective buffer of the plurality of buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in the respective buffer, and

wherein, for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic, the beginning and end data for the memory access request being [[and]] stored in the ~~single~~ respective sub-buffers ~~buffer~~ by the memory interface, the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data, and

wherein the control logic records a value of a pointer indicating a first sub-buffer of the single buffer storing the end data, such that the control logic is able to return to the indicated sub-buffer to retrieve the end data from the single buffer.

14.   (Previously Presented) A memory controller as recited in claim 1, wherein each of the plurality of buffers is a sub-buffer of a larger memory buffer in the memory interface.

15.   (Canceled)

16.   (Previously Presented) A method as recited in claim 7, wherein each of the plurality of buffers is a sub-buffer of a larger memory buffer in the memory interface.

17.   (Canceled)